摩西尔 Mooncell

PRODUCT SPECIFICATION

V4.0 | ENGLISH

C12S

ULTRA-COMPACT
LED RECEIVING CARD

100 Mbps bidirectional receiver for LED grid and strip displays

96 x 512	24 / 8	100 Mbps	24 / 48 VDC
MAX. PIXEL LOAD	SERIAL / RGB GROUPS	BIDIRECTIONAL LINK	POWER INPUT

COMPACT FORM · FLEXIBLE OUTPUT MAPPING · REDUNDANT RING

Online firmware upgrade | RGB gamma | Calibration | 90-degree rotation

HARDWARE VERSION C12S (V1.2)

SECTION 01

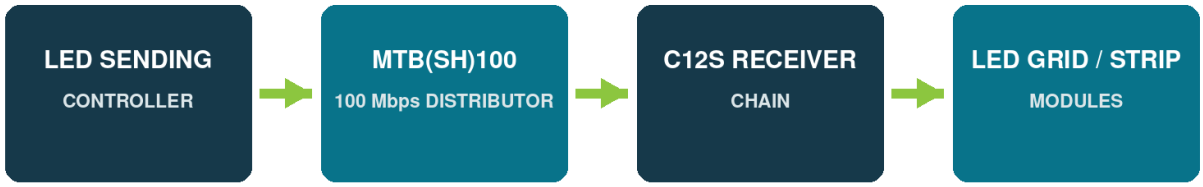
PRODUCT OVERVIEW

An ultra-compact LED receiving card for grid, strip and other space-constrained display structures.

The C12S is a compact Mooncell receiving card that supports 100 Mbps bidirectional communication, operating-status monitoring and a maximum load of 96 x 512 pixels (49,152 pixels). It is designed for architectural LED strip and grid-screen projects, as well as installations with strict space constraints.

96 x 512	24 / 8	<=256	1/1-1/4
PIXELS	DATA GROUPS	CARDS	SCAN SUPPORT
Maximum stated load	Serial / parallel RGB	Maximum cascade count	Released specification

SYSTEM ROLE



100 Mbps distribution and bidirectional receiver communication

PRODUCT CLASSIFICATION C12S is an LED receiving card. It operates downstream of an MTB(SH)100 100 Mbps distributor and outputs module data through P1 and P2.

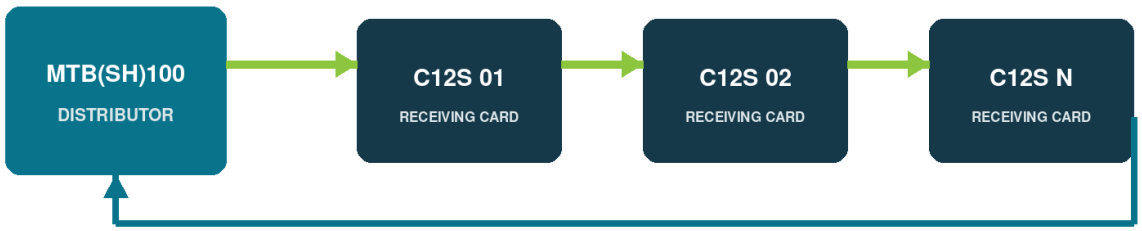
SECTION 02

COMMUNICATION & RELIABILITY

Bidirectional receiver communication, online maintenance and ring-redundant signal routing.

FUNCTION	ENGINEERING DESCRIPTION	APPLICATION VALUE
Bidirectional communication	Supports 100 Mbps bidirectional communication for display data and receiver-status readback.	Faster commissioning and diagnostics
Online firmware upgrade	Firmware can be upgraded online; the card restarts automatically after the upgrade without a power cycle.	Reduced service interruption
Fail-safe upgrade structure	Bootloader and application firmware are separated to improve upgrade safety.	Lower firmware recovery risk
Operating-status readback	Receiver operating status can be read back through the control system.	Remote maintenance visibility
Redundant ring	Primary and backup receiver links can be wired as a ring. If one path fails, the alternate path maintains display data.	Improved chain reliability
Simplified cabling	Signal transmission requires four conductors of Category 5e twisted-pair cable.	Lower cable and connector count

RECEIVER RING TOPOLOGY



Redundant return path closes the receiver ring

INTEGRATION NOTE The JP1 TX path accepts the 100 Mbps signal from the SH100 distributor; the RX path cascades the signal to the next C12S.

SECTION 03

DISPLAY & COMMISSIONING FUNCTIONS

Image-quality controls and configuration tools for conventional, PWM-driven and irregular LED structures.

FUNCTION	ENGINEERING DESCRIPTION	APPLICATION VALUE
Brightness calibration	Supports per-pixel brightness calibration and rapid calibration workflows.	Improves luminance uniformity
Chromaticity calibration	Supports per-pixel chromaticity calibration.	Improves color uniformity
Independent RGB gamma	With a compatible sending controller and software, red, green and blue gamma can be adjusted independently.	Helps correct low-gray non-uniformity and white-balance drift
Low-latency processing	Receiver-side processing delay can be reduced to as little as one frame for modules using driver ICs with built-in RAM.	Faster visual response
Display-mode priority	AutoLED 3.x or later provides refresh-rate-priority and grayscale-priority modes.	Balances refresh performance and grayscale depth
Image rotation	A receiver card can rotate its assigned image by 0, 90, 180 or 270 degrees.	Supports rotated cabinets and modules
Per-card image offset	The display position assigned to an individual receiver can be offset as required.	Supports irregular screen geometry
Driver-IC compatibility	New-generation image-processing architecture and broad LED driver-IC compatibility.	Flexible module integration

CONFIGURATION WORKFLOW

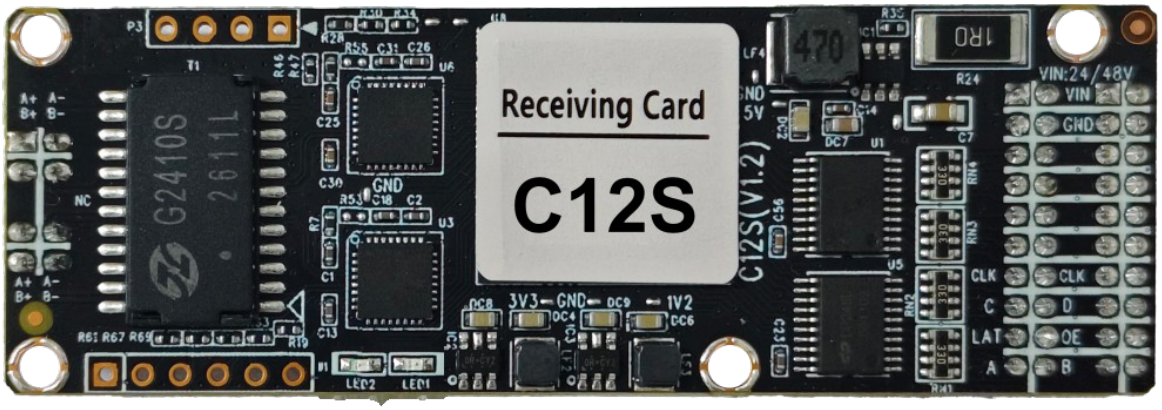
- Customize and inspect receiver output-data mappings in AutoLED 3.x or later.
- Arrange cabinets freely in Advanced Layout to build complex cabinet structures.
- Arrange cabinet connections in Complex Screen Connection to build irregular large-format screens.

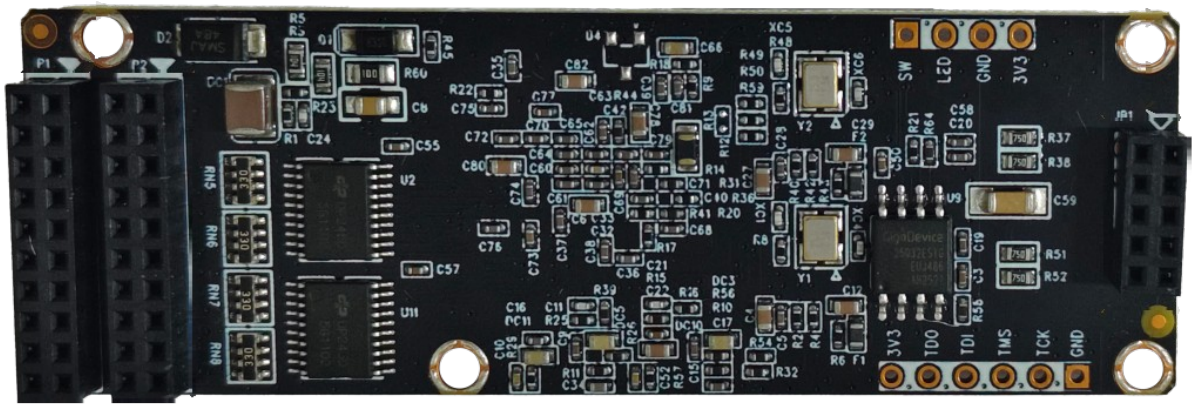
SOFTWARE COMPATIBILITY Functions that depend on AutoLED require a compatible released version and corresponding sending-controller support.

SECTION 04

BOARD LAYOUT & INTERFACES

Compact 77.5 x 26 mm receiver with two module-output connectors, status LEDs and one 100 Mbps link connector.





Product image is for reference only. The delivered hardware governs.

INTERFACE	ROLE	DESCRIPTION
P1 / P2	Module-data outputs	Carry serial or parallel RGB data and the 24/48 VDC supply rail, according to the configured firmware mode.
LED1	Green status LED	Reports receiver operation, network-data state and upstream DVI-source status.
LED2	Red power LED	Illuminates steadily when the receiver is powered normally.
JP1	100 Mbps signal connector	TX accepts the signal from SH100; RX cascades the signal to the next receiving card.

INTERFACE MODE P1 and P2 use different signal assignments in parallel-RGB and serial-output modes. Apply only the pinout for the active firmware configuration.

SECTION 05

STATUS INDICATORS & LINK BEHAVIOR

LED1 reports receiver and upstream-source status; LED2 confirms normal receiver power.

INDICATOR	STATE	MEANING
LED1 - green	Uniform slow flash	Receiver operating normally; 100 Mbps link/data normal; no upstream DVI source signal.
LED1 - green	Uniform fast flash	Receiver operating normally; 100 Mbps link/data normal; upstream DVI source signal present.
LED1 - green	Off	No network data/link signal.
LED1 - green	Two fast flashes every 4 s	Receiver is in bootloader mode.
LED2 - red	Steady on	Receiver power supply is normal.

FIELD CHECK SEQUENCE

- Confirm LED2 is steadily illuminated to verify power.
- Observe LED1 for the 100 Mbps communication state.
- Use the slow/fast flash rate to identify whether the upstream DVI source is absent or present.
- If LED1 gives two fast flashes every four seconds, the card is in bootloader mode.

LINK BEHAVIOR

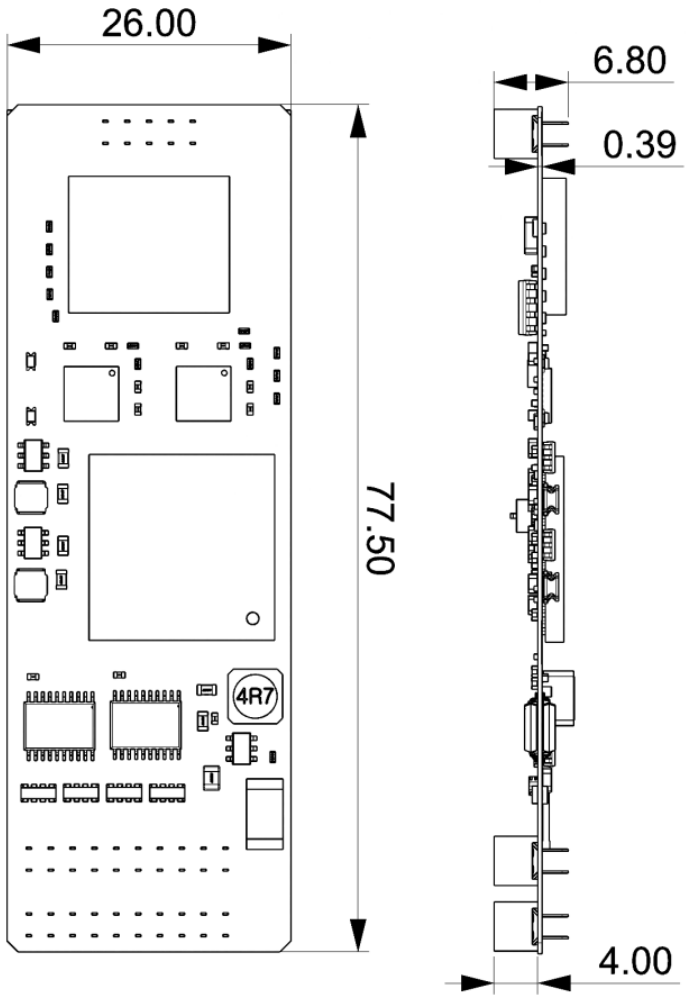
Receiver cards may be cascaded through JP1. In a redundant-ring installation, primary and backup paths are both connected so that a single link failure does not interrupt display data.

TERMINOLOGY The DVI indication refers to the upstream video-source state distributed through the LED control system; C12S itself has no DVI connector.

SECTION 06

MECHANICAL DIMENSIONS

Ultra-compact board geometry for LED grid, strip and space-constrained display structures.



Dimensional tolerance: +/-0.3 mm. Units: mm.

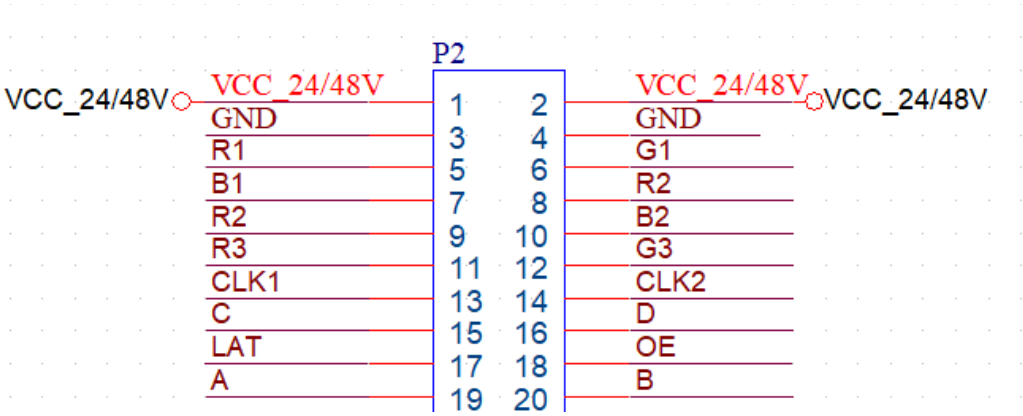
PARAMETER	VALUE	REFERENCE
PCB outline	77.5 x 26.0 mm	Length x width
Front-side profile	6.80 mm	Maximum dimension shown in the released drawing
Rear-side profile	4.00 mm	Maximum dimension shown in the released drawing
PCB thickness reference	0.39 mm	Dimension shown in the released drawing
Net weight	12 g	One receiving card

MECHANICAL INTEGRATION Reserve adequate clearance around P1, P2, JP1 and the component-side profiles. Verify the production hardware before finalizing cabinet tooling.

SECTION 07

PARALLEL RGB OUTPUT - P2

P2 carries RGB groups 1-3, timing/control signals and the receiver supply rail in parallel-output mode.



Connector: dual-row female, 2 x 10 positions, 2.0 mm pitch, straight (180 degrees).

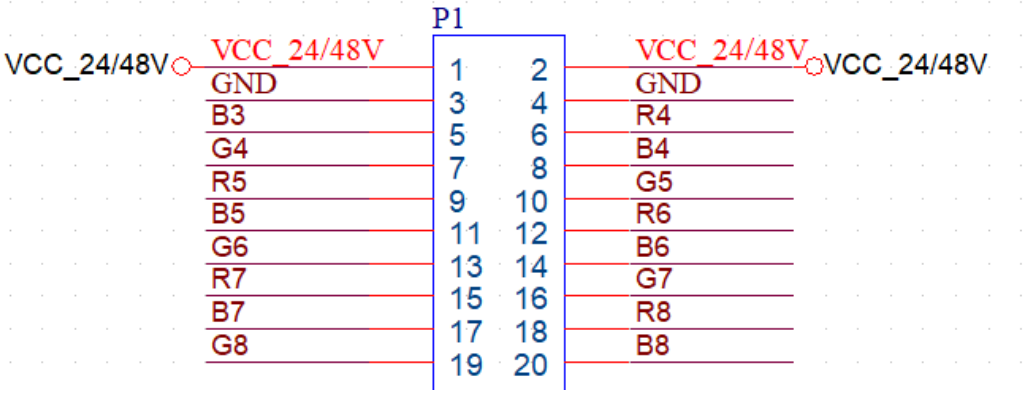
FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION
24/48 VDC rail	VCC	1	2	VCC	24/48 VDC rail
Ground	GND	3	4	GND	Ground
RGB parallel data	R1	5	6	G1	RGB parallel data
RGB parallel data	B1	7	8	R2	RGB parallel data
RGB parallel data	G2	9	10	B2	RGB parallel data
RGB parallel data	R3	11	12	G3	RGB parallel data
Shift clock 1	CLK1	13	14	CLK2	Shift clock 2
Clock 3 / row C	CLK3 / C	15	16	CLK4 / D	Clock 4 / row D
Latch	LAT	17	18	OE	Output enable
Row address	A	19	20	B	Row address

SUPPLY LABEL The released connector schematic identifies P2 pins 1 and 2 as VCC_24/48V; this English table follows that schematic.

SECTION 07

PARALLEL RGB OUTPUT - P1

P1 carries RGB groups 3-8 and the receiver supply rail in parallel-output mode.



FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION
24/48 VDC rail	VCC	1	2	VCC	24/48 VDC rail
Ground	GND	3	4	GND	Ground
RGB parallel data	B3	5	6	R4	RGB parallel data
RGB parallel data	G4	7	8	B4	RGB parallel data
RGB parallel data	R5	9	10	G5	RGB parallel data
RGB parallel data	B5	11	12	R6	RGB parallel data
RGB parallel data	G6	13	14	B6	RGB parallel data
RGB parallel data	R7	15	16	G7	RGB parallel data
RGB parallel data	B7	17	18	R8	RGB parallel data
RGB parallel data	G8	19	20	B8	RGB parallel data

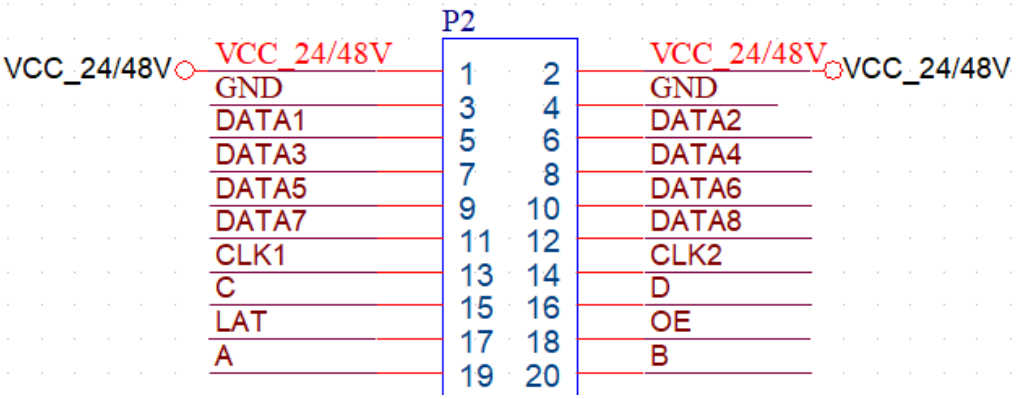
CLOCK AND ROW-ADDRESS RULES

- With 5958 decoding drivers: A is DCLK, B is BK and C is DIN.
- With four expanded clock groups, use only A and B for scan addressing; P2 pins 15 and 16 carry CLK3 and CLK4 (standard firmware).
- When A, B, C and D are required for scan addressing, only two clock groups are available; P2 pins 15 and 16 carry C and D (custom firmware).

SECTION 08

SERIAL OUTPUT - P2

P2 carries serial DATA1-DATA8, timing/control signals and the receiver supply rail in serial-output mode.



Connector: dual-row female, 2 x 10 positions, 2.0 mm pitch, straight (180 degrees).

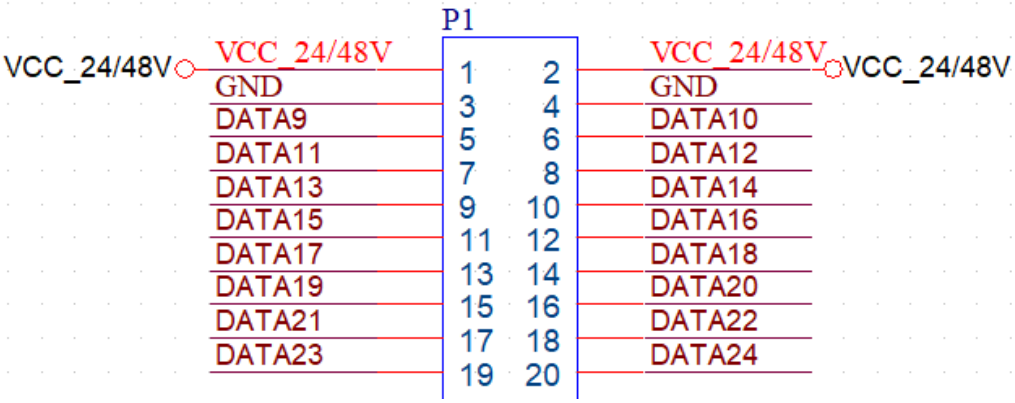
FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION
24/48 VDC rail	VCC	1	2	VCC	24/48 VDC rail
Ground	GND	3	4	GND	Ground
Serial data	DATA1	5	6	DATA2	Serial data
Serial data	DATA3	7	8	DATA4	Serial data
Serial data	DATA5	9	10	DATA6	Serial data
Serial data	DATA7	11	12	DATA8	Serial data
Shift clock 1	CLK1	13	14	CLK2	Shift clock 2
Clock 3 / row C	CLK3 / C	15	16	CLK4 / D	Clock 4 / row D
Latch	LAT	17	18	OE	Output enable
Row address	A	19	20	B	Row address

MODE CONTROL Serial and parallel assignments are mutually exclusive firmware modes. Confirm the active receiver program before wiring the module harness.

SECTION 08

SERIAL OUTPUT - P1

P1 carries serial DATA9-DATA24 and the receiver supply rail in serial-output mode.



FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION
24/48 VDC rail	VCC	1	2	VCC	24/48 VDC rail
Ground	GND	3	4	GND	Ground
Serial data	DATA9	5	6	DATA10	Serial data
Serial data	DATA11	7	8	DATA12	Serial data
Serial data	DATA13	9	10	DATA14	Serial data
Serial data	DATA15	11	12	DATA16	Serial data
Serial data	DATA17	13	14	DATA18	Serial data
Serial data	DATA19	15	16	DATA20	Serial data
Serial data	DATA21	17	18	DATA22	Serial data
Serial data	DATA23	19	20	DATA24	Serial data

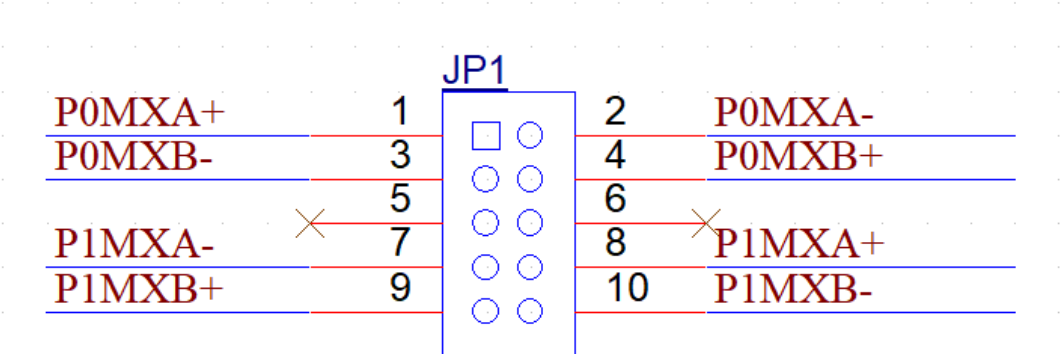
SHARED P2 TIMING RULES

- With 5958 decoding drivers: A is DCLK, B is BK and C is DIN.
- Four-clock expansion uses A/B row addressing and assigns P2 pins 15/16 to CLK3/CLK4.
- A/B/C/D row addressing limits clock expansion to two groups and assigns P2 pins 15/16 to C/D.

SECTION 09

100 MBPS LINK CONNECTOR - JP1

JP1 carries the bidirectional 100 Mbps input/cascade link between SH100 and the C12S receiver chain.



Connector: dual-row female, 2 x 5 positions, 2.0 mm pitch; positions 5 and 6 are unused.

PIN	SIGNAL	DESCRIPTION
1	P0MXA+	P0 channel differential pair A, positive
2	P0MXA-	P0 channel differential pair A, negative
3	P0MXB-	P0 channel differential pair B, negative
4	P0MXB+	P0 channel differential pair B, positive
5	NC	Not connected / keyed position
6	NC	Not connected / keyed position
7	P1MXA-	P1 channel differential pair A, negative
8	P1MXA+	P1 channel differential pair A, positive
9	P1MXB+	P1 channel differential pair B, positive
10	P1MXB-	P1 channel differential pair B, negative

PIN ORIENTATION This table follows the connector schematic in source V4.0. Confirm the PCB pin-1 marker and released harness drawing before cable fabrication.

SECTION 10

LOADING CAPACITY & SCAN SUPPORT

Performance limits for conventional and PWM-driven LED modules under the released C12S configuration.

DRIVER TYPE	MAXIMUM LOAD	BRIGHTNESS CALIBRATION	CHROMATICITY CALIBRATION
Conventional driver	96 x 512 pixels	96 x 512 pixels	96 x 512 pixels
PWM driver	96 x 512 pixels	96 x 512 pixels	96 x 512 pixels

OUTPUT AND SYSTEM LIMITS

PARAMETER	SPECIFICATION
Output-data modes	24 serial data groups / 8 parallel RGB data groups
Maximum cascade count	<=256 receiving cards
Scan support	1/1 to 1/4 scan
Maximum pixel count	49,152 pixels (96 x 512)
Supported driver categories	Conventional and PWM LED driver ICs

CAPACITY RULES

- Loading capacity is stated as receiver width x height; do not exceed the released 96 x 512-pixel limit.
- Brightness and chromaticity calibration use the same stated load limit as normal operation.
- The 24-serial-group and 8-parallel-group assignments depend on the selected output firmware mode.

NATIVE PIXEL ADDRESSING Configure the receiver's assigned pixel area and cabinet layout in AutoLED. Use native-resolution 1:1 pixel mapping where the application requires source pixels to map directly to LED pixels.

SECTION 11

GENERAL SPECIFICATIONS

Electrical, environmental, mechanical, packaging and compliance data for system integration and procurement.

CATEGORY	PARAMETER	SPECIFICATION
Electrical	Input voltage	24 / 48 VDC
Electrical	Rated current	24 V: 0.05 A / 48 V: 0.03 A
Electrical	Rated power	1.5 W
Operating environment	Temperature	-20 °C to +70 °C
Operating environment	Relative humidity	10% RH to 90% RH
Storage environment	Temperature	-25 °C to +125 °C
Mechanical	Board dimensions	77.5 x 26.0 mm
Mechanical	Net weight	12 g per card
Packaging	Outer carton	368 x 207 x 85 mm
Packaging	Gross weight	1.90 kg including cables and accessories
Packaging	Pack quantity	100 cards per carton
Compliance	Standards	RoHS compliant; CE-EMC compliant

POWER NOTE Current and power consumption may vary with operating conditions, environment and receiver configuration.

PROCUREMENT CHECKS

- Confirm the required 24 VDC or 48 VDC system supply before installation.
- Confirm the required serial or parallel output harness and firmware configuration.
- Verify carton quantity and accessory contents against the purchase order.

SECTION 12

INSTALLATION, SAFETY & DOCUMENT CONTROL

Installation requirements and revision traceability for the C12S hardware version V1.2.

INSTALLATION AND HANDLING

- Installation must be performed by qualified personnel.
- Use appropriate electrostatic-discharge precautions when handling the receiving card.
- Protect the product from water and dust during installation and operation.
- Confirm P1/P2 output mode, JP1 orientation and the 24/48 VDC supply before connecting the harness.

COMMISSIONING CHECKLIST

CHECK	ACCEPTANCE CONDITION
Power	LED2 is steadily illuminated after power is applied.
Communication	LED1 indicates normal 100 Mbps link/data behavior.
Video source	LED1 flash rate corresponds to the upstream DVI-source state.
Output mode	Serial or parallel pinout matches the active receiver firmware.
Display mapping	Assigned area, rotation and per-card offset are verified in AutoLED.
Redundancy	Primary and backup ring paths are tested where ring backup is used.

DOCUMENT CONTROL

DOCUMENT VERSION	HARDWARE VERSION	RELEASE DATE	CHANGE DESCRIPTION
V4.0	C12S (V1.2)	August 21, 2026	Initial document release

NOTICE Specifications and product appearance are subject to change without notice. Confirm current hardware and released documentation before deployment.

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Professional LED Display Control Systems